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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/044,777
Filing Date: January 11, 2002
Appellant(s): CHASON ET AL.

Steven G. Parmelee
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/5/04

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1 and 14-20 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7). Likewise, group 2 (claims 2-4, 21-28) stand and fall together, Group 3 (claims 5-8) stand and fall together; Group 4 (claims 9-11) stand and fall together; and Group 5 (claims 12-13) stand and fall together.

(8) Claims Appealed

A correct copy of appealed claims 1-28 appears on pages 9-13 of the appellant's brief. The Examiner requests that a copy of the claims be placed in an Appendix to the brief, rather than being placed within the brief.

(9) Prior Art of Record

6,335,571	Capote et al.	1-2002
5,258,648	Lin, Paul T.	11-1993
5,251,266	Spigarelli et al.	10-1993

EP 0 475 022 A1; Grube, Gary W. 03-1992

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

a. Claims 1 and 4-13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,335,571 to Capote et al. in view of U.S. Patent No. 5,258,648 to Lin.

Regarding claim 1, Capote discloses a method comprising: providing a semiconductor die (100, 10), and prior to placing the die on a printed wiring board (101, 20), disposing an underfill material (112, 37) on at least a portion of a second side thereof (figures 10-27).

Capote fails to disclose using an interposer with a semiconductor die attached to a first side thereof in place of using only a semiconductor die.

Lin discloses using an interposer (22) with a semiconductor die (12) attached to a first side thereof (figures 2 and 4; column 2, lines 39-65; column 3, lines 12-25; column 4, lines 49-68), rather than using only a semiconductor die, for attachment to a printed wiring board.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Capote, such that an interposer having at least one semiconductor die attached to a first side thereof is used in place of only a semiconductor die, as taught by Lin. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an interposer with a semiconductor die in place of just a semiconductor die for bonding to a PWB, because Lin teaches that using an interposer allows for the thermal expansion

compensation through use of an underfill disposed between the interposer and PWB, while still allowing a semiconductor die to be reworked or removed from the assembly (Lin, column 2, lines 39-65; column 3, line 55 – column 4, line 20). The combination of Capote and Lin allows a semiconductor die to be mounted on the PWB, burned in, tested, and removed if defective, without permanently attaching a defective die to the assembly (also see Lin, column 1, line 60 – column 2, line 21).

Regarding claims 4 and 5, Capote (as modified by Lin, supra) discloses the method steps of adding at least one interface electrode (30) to the second side of the interposer after disposing the underfill material (37; figures 19-21).

Regarding claim 6, Capote discloses disposing an underfill material on a portion of the second side thereof while simultaneously providing at least one aperture in the underfill material (column 10, lines 57-58; column 11, lines 18-21).

Regarding claim 7, Capote (as modified by Lin, supra) discloses adding at least one interface electrode (30) in the at least one aperture (figures 19-21).

Regarding claim 8, Capote discloses forming at least one aperture (38) in the underfill material (37), and adding at least one interface electrode (30) in the at least one aperture (figures 19-21).

Regarding claim 9, Capote discloses disposing an underfill including a plurality of material layers (column 4, lines 18 – 29; column 5, lines 10-36).

Regarding claims 10 and 11, Capote discloses exposing at least one of the material layers to low-temperature processing/drying (curing would inherently cause drying; column 12, lines 1-17; column 15, lines 1-7; column 5, line 32).

Regarding claim 12, Capote (as modified by Lin, supra) discloses removing at least a portion of the underfill material to expose at least a portion of at least one interface electrode (column 9, lines 59 – 62).

Regarding claim 13, Capote discloses using grinding or abrasion to expose the electrode (column 9, lines 59 – 62).

b. Claims 1-3, and 21-28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Capote et al.

Regarding claims 1, 21, and 25, Lin discloses a method comprising: providing at least one interposer (22) having at least one semiconductor die (12) attached to a first side thereof (figures 1-5; column 5, lines 1-40); providing a printed wiring board (34); and attaching the interposer to the printed wiring board and underfilling the area between the interposer and PWB (column 5, lines 15-40).

Lin fails to disclose disposing a pre-form underfill on the second side of the interposer, with an interface electrode at least partially exposed through the underfilling material.

Capote teaches the use and advantages of a pre-form underfill (112, 37) with partially exposed electrodes (14, 30) disposed on the second side of a circuit element, which is then attached to a printed wiring board (column 2, line 1 – column 3, line 38; column 6, lines 19-29; figures 13, 17, 21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method/device of Lin such that a pre-form underfill is

disposed on the interposer, as taught by Capote, rather than undergoing a process of underfilling. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to dispose an underfill material with partially exposed electrodes on the bottom of the interposer, because Capote teaches that conventional underfilling processes are generally disadvantageous, resulting in reduced production efficiency, increased production cost, increased production time, reduced reliability, and increased susceptibility to void formation or delamination (see Capote, column 2, line 48 – column 3, line 38). Capote then shows that the process of disposing an underfilling material on the component to be connected to the PWB, and then providing solder electrodes partially exposed through the underfilling, reduces or eliminates the problems with using a conventional underfilling method (see Capote, column 4, line 18 – column 6, line 30). Thus, it is well within the purview of a person having ordinary skill in the art to use the pre-formed underfill method taught by Capote in place of the conventional underfilling method, when attaching the interposer and chip of Lin on the PWB for the reasons listed supra.

Regarding claims 2, 3, 22, 26, and 28, Lin discloses that the interposer has solder balls (32) disposed on a second side thereof (figures 3 and 4; column 5, lines 3-14), the solder balls acting as a means for physically and electrically coupling the die to the PWB (figures 3 and 4).

Regarding claims 23 and 24, Lin fails to disclose further processing or heating the interposer on the PWB to at least partially harden the underfilling material.

Capote teaches heating of the interposer on the PWB to at least partially harden the underfilling material (column 9, lines 20-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Lin by heating the interposer on the PWB, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to heat the interposer/PWB assembly, because doing so cures the encapsulants, such that a continuous and voidless seal is formed between the PWB and chip component, as well as allow for the reflowing and connection of the solder joints of the chip component to the PWB (see Capote, column 9, lines 20-32). It is well within the purview of a person of ordinary skill to recognize that having a continuous seal between the components as well as fully reflowed solder joints improves the reliability of the assembly and provides protection for the assembly.

Regarding claim 27, Lin fails to disclose that the underfilling material comprises adherence means.

Capote teaches that the underfill comprises adherence means (column 8, lines 38-60; column 9, lines 20-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the underfilling material of Lin as modified by Capote, supra, comprises adherence means, as is further taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an underfilling material with adherence means, so that the

chip component is reliably attached and affixed to the PWB, as is appreciated by one skilled in the art.

c. Claims 14-18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Capote et al. as applied to claim 1 above, and further in view of European Patent Publication No. 0 475 022 A1 to Grube et al.

Regarding the claims, Lin fails to disclose providing a plurality of interposers disposed substantially co-planar to one another in a panel arrangement, disposing an underfill material on at least a portion of the second side of some of the plurality of interposers, and then singulating the interposers.

Grube discloses providing a plurality of interposers disposed substantially co-planar to one another in a panel, wherein at least some of the interposers each have at least one semiconductor die attached to one side thereof (see column 2, lines 32-58), disposing an attachment material on at least a portion of the second side of at least some of the plurality of interposers (adhesive is provided on the entire interposer sheet; see column 5, lines 23-39), and then singulating the interposers to provide singulated interposers (column 6, lines 5-18; figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Lin as modified by Capote, so that an interposer sheet is used when attaching chips and disposing underfill material as suggested by Grube. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use an interposer sheet in

place of a singulated interposer, because doing so allows for the processing steps involved with chip attachment, via patterning, and adhesive deposition to be formed for multiple interposers in a single step, rather than requiring separate manufacturing steps for each interposer (see Grube, column 2, lines 30-58).

d. Claims 19 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Capote et al. and further in view of Grigg, as applied to claim 18 above, and further in view of U.S. Patent No. 5,251,266 to Spigarelli et al.

Lin fails to disclose placing singulated interposers into a matrix tray carrier to facilitate subsequent placement of the singulated interposers on a printed wiring board.

Spigarelli discloses placing singulated IC devices in a matrix tray carrier (column 4, lines 1-4) to facilitate subsequent placement of the singulated devices on a printed wiring board (column 8, lines 38-45; column 13, lines 37-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Lin as modified by Capote and Grube, such that singulated interposers are placed into a matrix tray carrier, as taught by Spigarelli. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to place the singulated interposers into a carrier, so that the carrier features can be utilized to determine the position of each interposer, and thus allow for greater accuracy of placement onto a printed wiring board (Spigarelli, column 13, lines 37-68) as well as allow for automated pick and place bonding to a printed wiring board (Spigarelli, column 8, lines 38-45; column 13, lines 37-68).

(11) Response to Argument

Regarding the Group 1 arguments:

The appellant first argues that "Capote does not teach providing a complete underfilling on either the die or the substrate alone. Rather, it is the final combination that provides sufficient material to actually fill the available space." In response to appellant's argument that Capote fails to teach a complete underfilling, it is noted that "a complete underfilling" is not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is also respectfully pointed out that Capote does teach an embodiment using a complete underfilling, such as that of figure 18 (also see column 5, lines 10-40; column 10, lines 12-35).

The Appellant further argues that a combination of Capote and Lin ignores the teachings of the Capote reference. The Appellant further states that Capote teaches that "interposers are to be used without an underfill material.... Interposers are set forth in Capote as being a satisfactory stand-alone solution. In short, Capote teaches that interposers and underfill materials are different, alternative approaches to reliably securing a die to a substrate."

The Examiner, however, submits that the teachings pertaining to interposers appearing in columns 1-2 of the Capote reference are merely a discussion of common prior art techniques for handling thermal expansion. As Capote teaches, conventionally, thermal expansion mismatches have been compensated by using an interposer between a chip and a wiring board, or by using an

underfill between a chip and a wiring board, both techniques having respective advantages and disadvantages, as is known in the art. Capote does not indicate that it would in any way be undesirable or inoperable to combine underfill and interposer technologies. Capote, in fact, makes no suggestion or teaching pertaining to a combination of underfill and interposer technologies. In order for Capote to lead a person to move in a fashion contrary to the explicit teachings of Capote, or to teach away from Capote, as the Appellant asserts, Capote would need to indicate in some way that the combination of technologies is undesirable. Merely mentioning that interposers have been used for thermal expansion mismatch does not sufficiently teach away from using interposers with the invention of Capote. Additionally, the discussion of interposer technologies in Capote only addresses one common type of interposer: that used without an underfill. Even if the invention of Capote does not suggest usage with the underfill-lacking interposer mentioned by Capote, it would be remiss to suggest that Capote teaches away from the usage of a pre-formed underfill with all interposer technologies. In the rejection of claim 1, Capote is combined with U.S. Patent No. 5,258,648 to Lin, which already teaches the combination of an interposer and an underfill, and thus, cannot be considered equivalent to the underfill-lacking interposer technology addressed by Capote.

Further, although the Examiner does not concede that Capote may teach away from combining underfill and interposer technologies, the Capote reference must be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art, including nonpreferred embodiments. Disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments (See MPEP 2123; *Merck & Co. v. Biocraft Laboratories*, 874 F.2d 804, 10 USPQ2d 1843, 493 U.S. 975 (1989); *In re*

Susi, 440 F.2d 442, 169 USPQ 423 (1971); *In re Gurley*, 27 F.3d 551,554, 31 USPQ2d 1130, 1132 (1994)). The primary teachings of Capote are the usage of a pre-form underfill on a chip component, rather than flowing an underfill material by capillary action, in order to improve upon disadvantages of the flown underfills, such as: high expense, inefficient processing, long processing time, formation of air bubbles in the underfill, low reliability, and high void formation (see Capote, column 2-3; particularly column 3, lines 15-38). Thus, it is the Examiner's opinion that a person having ordinary skill in the art would have been motivated to replace any capillary- flown underfill materials used in the prior art for bonding a chip component to a wiring board with a pre-formed underfill, in order to improve at least the cost, processing time, and processing efficiency, as is suggested by Capote. Since Lin teaches a structure using both an interposer and a capillary-flown underfill, it is the examiner's opinion that a combination of Lin and Capote, such that the more expensive and less efficient capillary-flown underfill is replaced by a pre-formed underfill, would have been reasonably suggested to one having ordinary skill in the art based on the teachings of Capote.

The Appellant even further argues with respect to a combination of Lin and Capote that "Lin makes no suggestion that the underfill material could or should be added to the interposer prior to disposing the interposer on the substrate. Furthermore, a combination of Lin and Capote, regardless of which reference is viewed as a starting point, fails to achieve the claimed invention... A forced combination of Capote and Lin is therefore likely to yield a structure wherein the die couples to the interposer with two underfill materials disposed therebetween and wherein another underfill material is added between the interposer and the substrate once those two structures have been joined."

The Examiner respectfully disagrees. Lin does teach a capillary-flown underfill between the interposer and the substrate, but Capote clearly shows that it is advantageous to use a pre-formed underfill, rather than a flown underfill, as is discussed supra. Also, since Capote teaches *replacing* a flown underfill material with a pre-formed material, then a combination of Capote and Lin would clearly involve *replacing* the underfill material of Lin with that taught by Capote, rather than adding another underfill layer, as is suggested by the Appellant.

Regarding group 2, the Appellant asserts that "neither Lin nor capote makes any teaching that an underfill material can be placed on an interposer in a way that accommodates such interface electrodes."

The Examiner disagrees. Lin teaches that interface electrodes (32) coupled on a second side of the interposer, for connection with a wiring board, wherein the interface electrodes are provided within the underfill material (see figures 4-5 of Lin). Capote teaches methods for providing interface electrodes on a chip component also having a pre-formed underfill present on the same side as the interface electrodes, as is discussed in the rejections supra. Since the combination of Capote and Lin, as in claim 1, involves disposing a pre-form underfill on an interposer, and since both Lin and Capote teach interface electrodes surrounded by underfill material, it would be reasonable for a person having ordinary skill in the art to look to the teachings of Capote for providing both interface electrodes and a pre-form underfill on the same surface.

Regarding group 3, the Appellant states that "neither Capote nor Lin, alone or in any reasonable combination, teach, suggest, or result in such configurations."

The Examiner respectfully submits that Capote teaches: subsequent placement of interface electrodes (see figures 19-21) for claim 5; placement of such electrodes in an aperture formed simultaneously with placement of the underfill (see column 10, lines 57-60; column 11, lines 18-21) for claim 6; placement of an electrode in such an aperture (figures 19-21) for claim 7; and forming an aperture (38) in the underfill, and adding at least one electrode in the aperture (figures 19-21) for claim 8. Again, since Capote teaches the means for providing interface electrodes with a pre-formed underfill, the combination of Capote and Lin would use such methods to provide the interposer interface electrodes through a pre-formed underfill.

Regarding group 4, the Appellant states that neither Capote nor Lin teaches the material of claims 9-11.

This is not persuasive, because Capote teaches: disposing an underfill having a plurality of layers (see column 4, lines 18-29; column 5, lines 10-36) for claim 9, and the use of low-temperature drying (column 5, line 32; column 12, lines 1-17; column 15, lines 1-7; noting that curing at about 165 degrees would constitute "low temperature drying") for claims 10 and 11.

Regarding group 5, the Appellant states that neither Capote nor Lin teaches the material of claims 12 and 13.

The Examiner disagrees, since Capote discloses removing a portion of the underfill to expose a portion of an interface electrode (column 9, lines 59-62) for claim 12, and using grinding or abrasion (see column 9, lines 59-62) for claim 13.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

jmd

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June 4, 2004

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